

**Amendments to the Drawings:**

The attached sheet of drawings includes changes to Fig.2. This replacement sheet, which includes Fig. 2, replaces the original sheet including Fig. 2. In Figure 2, previously omitted elements 214 and 234 have been added. Another replacement sheet, which includes Fig. 6, replaces the original sheet including Fig. 6. In Figure 6, the proper text of 'reconfiguration data engine test' now appears in the box with the reference identifier of 620.

Attachment:Replacement Sheet

## **REMARKS**

Reconsideration of this application, as amended, is respectfully requested.

Claims 22, 23, 25, 26, and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Anand. Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Anand in view of Rona (US Pat. 5,350,940). Claims 1, 3, 4, 12, 27, 29, 30, and 32 are allowed. Claims 2, 6-11, 13, 15-19, 21, and 28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 2, 5, 6, 7, 8, 10, 11, 13, 15, 16, 21, 22, 27, 33, 35 and 37 have been amended.

### **Drawings**

The drawings are objected to because the following were left out or mis-labeled , reference number fuse box 214, redundant components should be labeled 2\_4, memory 332 referenced on page 12, paragraph 21 should be memory 330, and the text "reconfiguration data engine 610" should replace a "Self Test and Repair Processor" 610 in Fig. 6.

Applicant's amended the text and drawings corresponding to the above change requests.

### **Claim Objections**

Claims 5, 6, 8, and 22 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicants traverse the office actions assertion but nonetheless have further limited

claims 5, 6, and 8 to eliminate the office action's concerns.

Claims 33-38 stand rejected under 35 U.S.C. 101 because the specification states a machine readable medium could embody carrier waves, infrared signals, or digital signals. Applicants have amended the specification to eliminate the office action's concerns.

Claims 2, 6, 7, 9-11, 13, 15-19, 21, 28, 31 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The office action states "Claim 2 recites that "the repair data is a fuse box located external to the two or more memories. It is unclear how data could be a fuse box because data is not hardware." Amended claim 2 states "the repair data is in a fuse box located on the same chip but external to area occupied by the two or more memories." Amended claim 2 should clear up the office action's concern. Applicants request that the objections to claim 2 be withdrawn.

The office action states "Claim 6 recites, "the processor further includes logic configured to compress an amount of bits making up the actual repair signature'. It is unclear whether the compressed repair signature of claim 1 is the same as an actual repair signature. Claim 7 is similarly rejected. Based on Applicant's disclosure, a compressed repair signature is an actual repair signature and therefore claim 6 is repeating what was recited in claim 1 and fails to further limit the subject matter of a

previous claim.” Several other claims have similar objections.

However, paragraph 0021 from Applicant’s specification describes one possible embodiment of a concatenated repair signature, an actual repair signature and a dummy repair signature. Paragraph 0021 states

[0021]

The processor 310 contains redundancy allocation logic to execute one or more repair algorithms to generate a **repair signature** for each memory. The repair data container may be a fuse box 314. The fuse box 314 stores **actual repair signatures** for each memory having one or more defective memory cells and **dummy repair signatures** for each memory with no defective memory cells. The **concatenated repair signature** may be an aggregation of all the **repair signatures** for each of the memories connected to that processor 310. The processor 310 contains logic configured to compose a **concatenated repair signature** for all of the memories 302-330 sharing the processor 310 and the fuse box 314. The processor 310 composes a **concatenated repair signature** in order to store that **concatenated repair signature** in the fuse box 314. The processor 310 also contains logic configured to decompose the **concatenated repair signature** to send reconfiguration data into all of the memories 302-330 sharing the fuse box 314.

Amended claim 6 further defines an embodiment of the actual repair signature as: the actual repair signature is generated for each memory having one or more defective memory cells that were actually detected during fault testing.

Amended claim 8 further defines an embodiment of the concatenated repair signature as: the concatenated repair signature is a compilation of repair signatures for the two or more memories stored in the same repair data container and is stored in a format dependent upon whether one or more defective memory cells were detected during fault testing for that particular memory of the two or more memories.

Amended claim 10 further defines an embodiment of the dummy repair

signature as: a dummy repair signature is generated for each memory with no defective memory cells in which the field consists of the single bit that identifies the memory.

Thus, in these example embodiments an actual repair signature and a dummy repair signature differ based on whether the corresponding memory has a defect to be repaired or not and the concatenated repair signature derives its potential repair data based on the actual or dummy repair signature for each memory having its repair signature stored in the same repair data container. Applicants request that the objections to claims 6, 7, 9, and 17 be withdrawn.

The office action states "Claim 10 recites, 'wherein the repair data container stores indicator bits for each memory sharing that repair data container. It is unclear what 'that repair container' is referring to. The phrase 'that repair container' implies that there are multiple repair containers." There could be multiple repair data containers and nothing limits the claim to a single repair data container except applicant's amended the claim to read the repair data container which refers to the earlier instance of the repair data container. Applicants request that the objections to claim 10 be withdrawn.

The office action states "Claim 11 recites, 'wherein the fuse box has a dedicated field for each memory sharing that fuse box'. It is unclear what 'that fuse box' is referring to. The phrase 'that fuse box' implies that there are multiple fuse boxes." There could be multiple fuse boxes and nothing limits the claim to a single fuse box except applicant's amended the claim to read the fuse box which refers to the earlier instance of the fuse box. Applicants request that the objections to claim 11 be withdrawn.

The office action states "Claim 13 recites 'compression/decompression logic

around the repair container. It is unclear whether compression/decompression logic is compression logic or decompression logic; or whether it is compression logic and decompression logic. Furthermore, the term "around" is a relative term which renders the claim indefinite. The term "around" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear what distance the compression/decompression logic must be from the repair data container in order to be considered to be "around" the repair data container." Claim 13 as amended recites the compression/decompression logic is external to the repair data container and is configured to compress an amount of bits making up the actual repair signature and decompress an amount of bits making up the actual repair signature. The compression/decompression logic is configured to both compress an amount of bits making up the actual repair signature and decompress an amount of bits making up the actual repair signature. Applicants request that the objections to claim 13 be withdrawn.

The office action states "Claim 15 recites, "two or more processors including the first processor and a second processor". The closed-ended term "including" implies that there are no processors other than the first processor and the second processor. Therefore the recitation "two or more processors" is unclear. Claim 15 further recites, "coupled to one or more memories". It is unclear whether the "one or more memories" are the same memories in claim 1. Claim 21 is similarly rejected. Applicants disagree with the office actions interpretation of the word including. However, to make this a moot point applicants added the words at least in claim 21. Applicants also added "memories connected to the second processor [are] discrete from the memories coupled to the first processor to eliminate any issues there. Applicants request that the objections to

claims 15 and 21 be withdrawn.

The office action states "Claim 16 recites, "to generate an augmented repair signature". It is unclear what element is augmented to the repair signature. Amended claim 16 states the augmented actual repair signature has repair signature data to repair defects detected prior to the operation of the chip as well as defects detected during the initialization cycle of operation of the chip. Applicants request that the objections to claim 16 be withdrawn.

The office action states "Claim 18 recites, "wherein the processor also contains redundancy allocation logic and is coupled to the repair data container. It is unclear whether the processor is coupled to the repair data container; or whether the redundancy allocation logic is coupled to the repair data container." Claim 16 states that the processor contains logic to test a memory. Claim 18 then say the processor also contains redundancy allocation logic. The processor then couples to the repair data container. Applicants hope this explanation clear up any confusion. Applicants request that the objections to claim 18 be withdrawn.

Claims 22, 23, 25, 26, and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Anand. The office action states "regarding the newly amended limitations of claim 22, it is noted that the specific features recited are intended use, and do not limit the apparatus claimed to any specific structure." Applicants disagree. Claim 22 states wherein the fuse box contains an amount of non-volatile fuses to provide actual repair capability for only a subset of all of the memories that share the fuse box. This limitation defines a physical/structural amount of fuses contained in the

fuse box rather than some intended use. The physical amount of fuses a device contains is undeniably a structural limitation. This structural limitation in claim 22 is not addressed by the office action in making a proper 103 rejection. As such, a complete office action on the merits of claim 22 has not yet be given. Therefore, applicants request a substantive examination on the merits of claims 22, 23, 25, 26, and 33 and remind the examiner that the next office action must be treated as a first examination on this set of claims.

## **Conclusion**

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. A two month extension of time is submitted with this response. Applicants reserve all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge them to our Deposit Account No. 50-2191. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,  
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